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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,987	03/08/2002	Hajime Seki	302-001	7219

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,987	SEKI, HAJIME	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2006 and 10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamdani (patent No. 6,311,261) in view of Reinman etal (article entitled Classifying Load and Store Instructions for Memory Renaming) and Moudgill etal. (article entitled Register Renaming and Dynamic Speculation: and Alternative Approach).

3. Chamdani taught the invention substantially as claimed including a data processing ("DP") system comprising:

4. Microprocessor (RS/6000) based on superscalar architecture capable of out-of-order execution (e.g., see col. 5, lines 1-39), comprising: physical registers (e.g., see col. 11, lines 24-40); a free list (e.g., see fig.2) that is designated to hold unallocated physical-register numbers; and a mapping table (e.g., see fig. 2 and col. 29, lines 1-13) having entries that are provided in respective correspondence with a predetermined number of logical registers, said entries being each designated to hold a physical-register number; a method for performing register renaming in a pipelined manner, for each group of instructions that are to go through a process of register renaming simultaneously.

5. Chamdani did not expressly detail the same tag for load and store instructions.

6. Reinman taught the memory renaming using tags between load and store instructions (e.g., see p. 401, col. 2) where the load and store associated with the same address are assigned the same tag (e.g., see figs. 1, 2 and col. p.401 col. 2, last paragraph-col. 402, col. 1, first full paragraph). It is inherent that the register names are stored as a number (ones and zeros). This meets (the claimed step (a)) Associating each logical-register number shown as a destination operand with a tag based on the order of the instructions in a group [which corresponds to the store instruction], and associating each logical-register number shown as a source operand[which corresponds to the load instruction] that is RAW (read-after-write)[in the sequence of instructions in figure 2 the load with the tag=5 was after the store instruction with a tag=5] dependent on an instruction of the group with the same tag with which the destination operand of said instruction is being associated.

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Chamdani and Reinman. Both references were directed toward the renaming of instructions to provide out-of-order execution of instructions. One of ordinary skill would have been motivated to incorporate the Reinman teachings of tagging load and store instructions at least to detection and correction of data due to out of order execution hazards between load and store instructions.

8. Chamdandi did not expressly detail (step b). Moudgill however taught (e.g., see p. 204, col.2) The map table in the RS/6000 keeps track of mapping of logical register names to physical registers, and source register names a every instruction are renamed using the map; and the instruction's output register is mapped to a new free physical

register and a map is updated displacing register mapped by the output register. Moudgill taught (p. 205, col. 1) that the mapping table has an entry for each register name which contains a physical register currently associated with or mapped by the register name. There is a free pool of physical registers used to provide new physical registers when necessary. The output register name is mapped to some new physical register allocated from the free pool. This meets the claimed step (b) consisting of Renaming each logical-register number associated with a tag to the physical-register number that is taken out of said free list and is allocated in correspondence with the associated tag, and renaming each logical-register number associated with no tag to the physical-register number that is obtained by accessing said mapping table [the use of tags in Reinman for certain for load and store instruction and the mapping of all instructions currently associated with a register name by Moudgill using a mapping table, and allocating from the free list].

9. It would have been obvious to one of ordinary skill to combine the teachings of Chamdani and Mougill. Both references taught aspects of the RS/6000 system and therefore one of ordinary skill would have been motivated to incorporate the teachings of Moudgill at least to fully implement the register renamingfeatures of the RS/6000 and to expand the operation using the aspects of the RS/9000 that extends the floating point renaming to all registers (e.g., see p. 204, col. 2, of Moudgill).

10. As the length of steps a and b above, claim 4, claims step (a) takes multiple cycles and step (b) takes one cycle. As to the number of cycles since the Chamdani and Moudgill and Reiman teachings performed the same operations a the claimed

operations it would have been obvious to one of ordinary skill that the number of cycles required would have been the same as the claimed steps. On the other hand since step one involves the two instructions at different slots in a program sequence then the associating of two instructions that are decoded a different times would have not occurred simultaneously and therefore would have required multiple cycles (e.g. see fig. 2, also since the comparison of tags for determining the situation of the same tag for load and store would have occurred after associating load and store tags this further indicates that the step (a) would have required multiple cycles). As to step (b) since the renaming of Moudgill is performed using the mapping table that accesses free registers and this operation has no requirement of sequential operation then for each instruction step (b) would have required only one cycle (see the discussion above).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pentovski (patent No. 6,185,671) disclosed a system for checking data type of operands specified by an instruction using attributes in a tagged array architecture (e.g., see abstract).

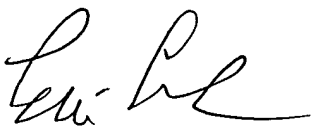
Meyer (patent No. 6,442,677) disclosed a system for superforwarding load operands in a microprocessor (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER